

SPU Block Diagram

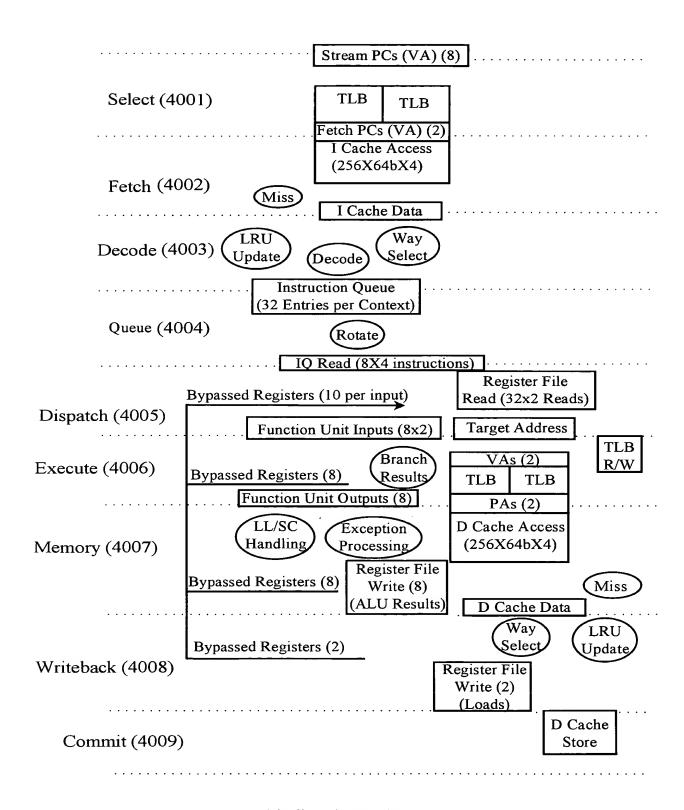
Fig. 1

New LRU bits

2-MRU-3	N/C	N/C		0	N/C		0		0	×
1-MRU-3	N/C	1	N/C	0	1	N/C	0	1	×	0
1-MRU-2	N/C		0	N/C		0	N/C	×	1	0
0-MRU-3		N/C	N/C	0	-		×	N/C	0	0
0-MRU-2	-	N/C	0	N/C	1	×		0	N/C	0
0-MRU-1		0	N/C	N/C	×	-	-	0	0	N/C
Way Accessed	0		2	3	0,1	0,2	0,3	1,2	1,3	2,3

Fig. 2

Function Unit Dispatch Pattern



Pipeline Timing Diagram Fig. 4

6 5 0	XSTREAM 110111	XSTREAM 110111		
	00000	STX 00001		
15 11 10	MASK	MASK		
21 20 16 15	RT	RT		
26 25 21	RS	RS		
31 26	Special 0000000	Special 0000000		

Masked Load/Store Instructions

Fig. 5

0	0		
31 Byte Pattern Mask	31 Register Start Mask	End of Mask	

LDX/STX Mask Registers

5 0	XSTREAM 110111	XSTREAM 110111
11 10 6 5	ADDX 00010	SUBX 00011
16 15 11	RD	RD
21 20 16	RT	RT
26 25 21	RS	RS
31 26	Special 0000000	Special 0000000

Special Arithmetic Instructions

	EAM 1111
2	XSTREAN 110111
9	
	SIESTA 00100
0	
	COUNT
2	
6 25	
26 25	SPECIAL 0000000

Siesta Instruction

Fig. 8

5 0	XSTREAM 110111	XSTREAM 110111		
11 10 6 5	GETSPC 10000	FREESPC 10001		
	RD	00000		
20 16 15	00000	00000		
26 25 21 20	RS	RS		
31 26	Special 0000000	Special 0000000		

PMU - Packet Memory Instructions

_								
5 0	XSTREAM 110111							
11 10 6	PKTEXT 10010	PKTINS 10011	PKTDONE 10100	PKTMOVE 10101	PKTUPD 10110	PKTPR 10111	PKTMAR 11010	PKTACT 11011
15	00000	RD	00000	00000	00000	ITEM	00000	RD
20 16	00000	RT	RT	RT	RT	RT	RT	000000
26 25 21	RS							
31 26	Special 0000000							

PMU - Queuing System Instructions

Fig 10

0			
5	XSTREAM 110111	XSTREAM 110111	
10 6 5	RELEASE 11000	GETCTX 11001	
15 11 10	00000	RD	
21 20 16 15	00000	00000	
26 25 21	00000	RS	
31 26	Special 0000000	Special 0000000	

PMU - RTU Instructions

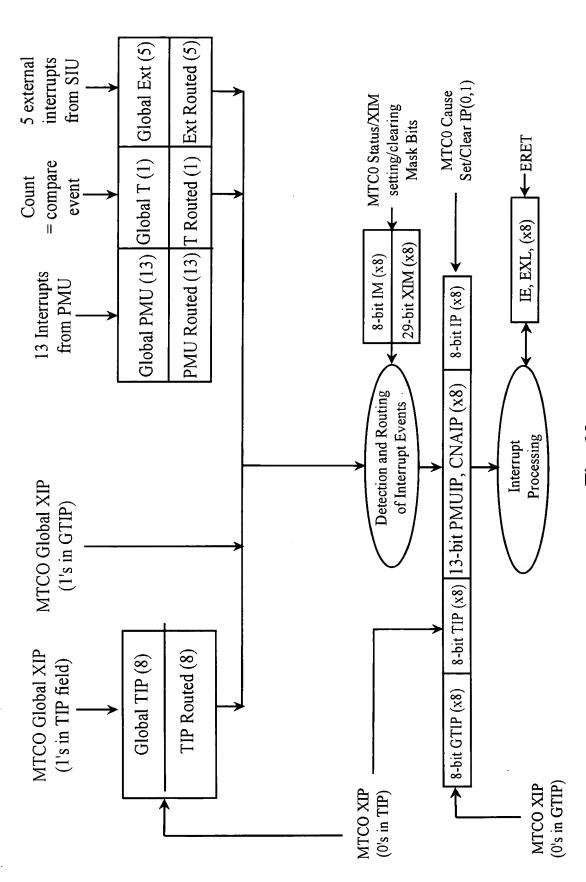
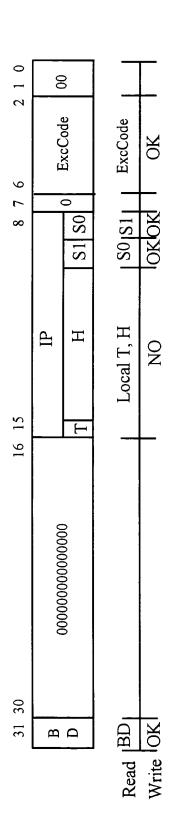


Fig. 12

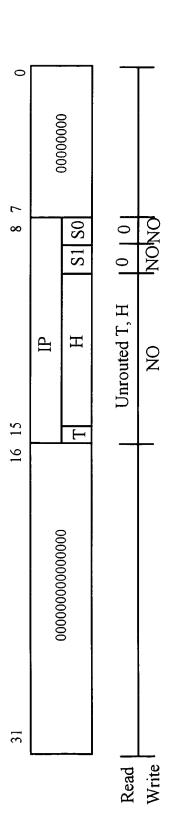
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Status Register



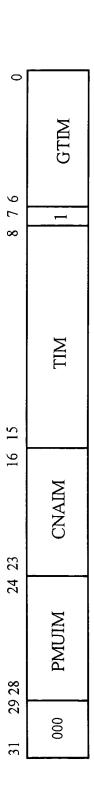
Cause Register

Fig. 14



Global Cause Register

Fig. 15



**Extended Interrupt Mask Register** 

7	GTIP	
15 8	TIP	
23 16	CNAIP	
29 28 24	PMUIP	
31 29	000	

Extended Interrupt Pending Register

Clear Selected Bits

Clear Selected Bits

%

N<sub>o</sub>

Local TIP

Local PMUIP | Local CNAIP

Read Write

Local GTIP

Fig. 17

7	GTIP	
15 8	TIP	
23 16	CNAIP	
29 28 24	PMUIP	
31 29	000	

Global Extended Interrupt Pending Register

| Deliver Selected Interrupts

Deliver Selected Interrupts

N<sub>o</sub>

No

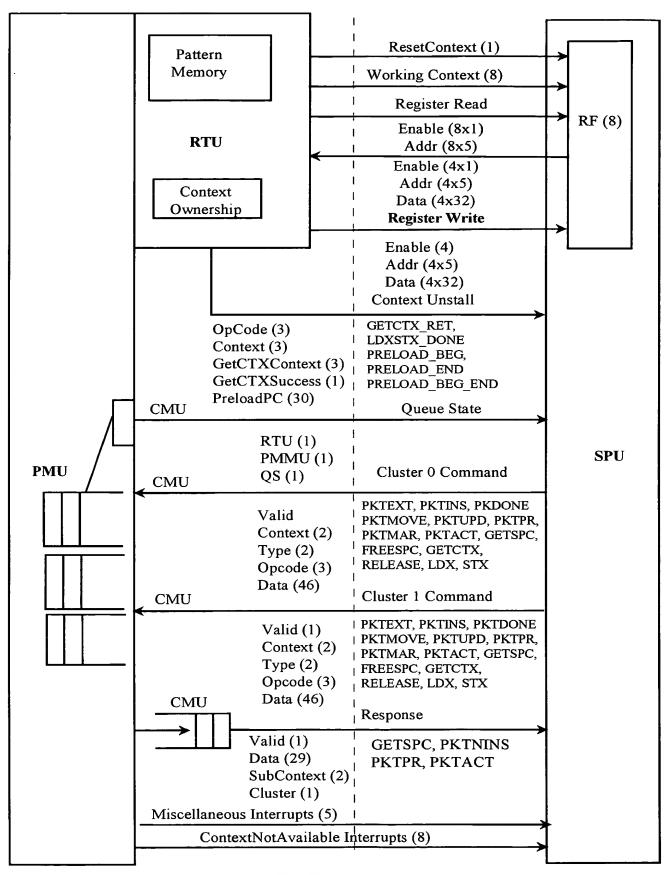
Unrouted TIP

Unrouted PMUIP Unrouted CNAIP

Read Write

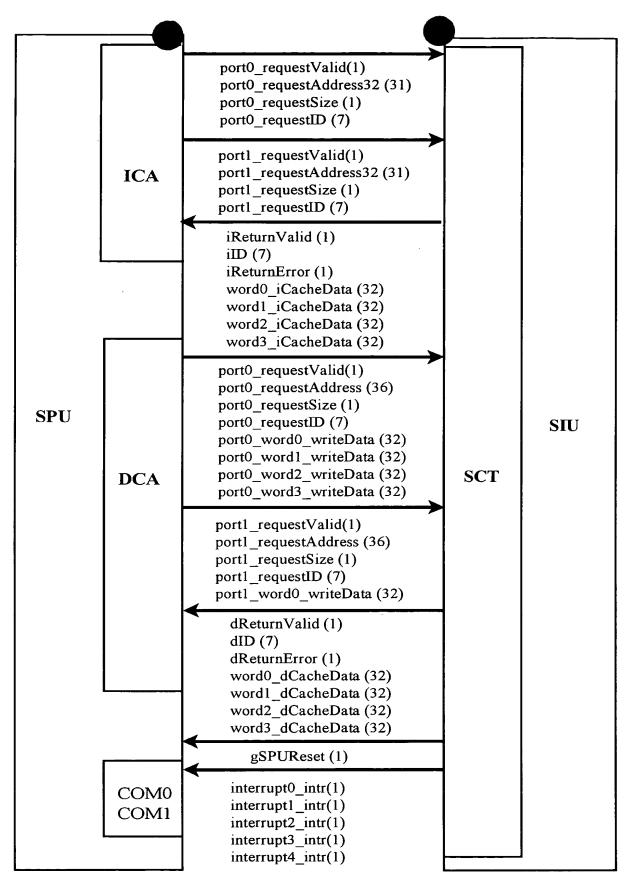
00000000

Fig. 18



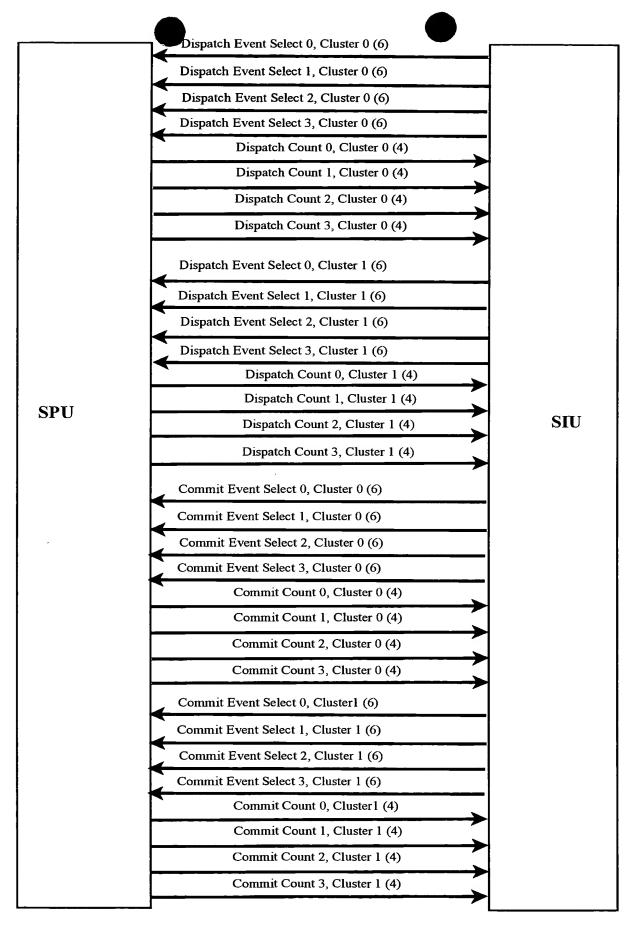
PMU/SPU Interface

Fig. 19



SIU/SPU Interface

Fig. 20



Performance Counter Interface Fig. 21

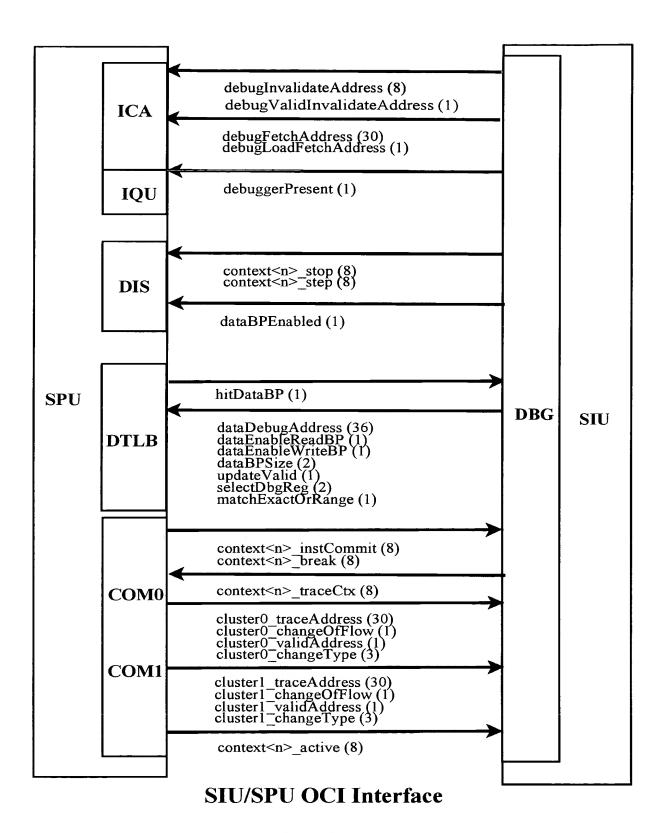


Fig. 22

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	<b>BEV</b>	Cause	Virtual Address	Physical Address	Memory Type
	1	Reset	BFC00000	01FC00000	uncached
	1	TLB Refill	BFC00200	01FC00200	uncached
(Ti	1	General	BFC00380	01FC00380	uncached
£)	0	TLB Refill	80000000	000000000	determined by KO
	0	General	80000180	0000000180	determined by KO
	0	XCInterrupt	80000480	0 000000480	determined by KO
₽	0	Activation	(VA Configurab	le within the PMU)	

## **XCaliber Vectors**

Fig. 23

Exceptions	Cause Code
Address Error - Instruction	4
Address Error - Data Load	4
Address Error - Data Store	5
TLB refill - Instruction	2
TLB invalid - Instruction	2
TLB refill - Data Load	2
TLB refill - Data Store	3
TLB invalid - Data Load	2
TLB invalid - Data Store	3
TLB modify - Data Store	1
Bus error - Instruction	6
Bus error - Data	7
Integer overflow	12
Trap	13
System Call	8
Breakpoint	9
Reserved instruction	10
Coprocessor unusable	11
Watch	23
Interrupt	0
XC Interrupt	0

**List of Vector Exceptions** 

Fig. 24

Context Number Register

## 0 K0 3 2

31

Config Register

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	Current State	SIU Input	Dispatched one instruction this cycle	Next State
	Run	Run	X	Run
		Idle	X	Idle
14		Step	X	Stop
u: M	Run Idle	Run	X	Run
ı <u>D</u>		Idle	X	Idle
M		Step	X	Step
#   <b>-1</b>	Step	Run	X	Run
		Idle	X	Idle
		Step	0	Step
÷		Step	1	Step_Idle
	Step Idle	Run	X	Run
		Idle	X	Idle
		Step	X	Step Idle

## **Operation of the OCI State Machine**

Bit Value	<b>Type</b>
000	Branch Not Taken
001	Branch Taken
010	JMP, ERET
011	Exception - TLB Refill
100	Exception - General Exception
101	Exception - Packet Load Exception
110	Exception - Extended Interrupt
111	Invalid

Fig. 28

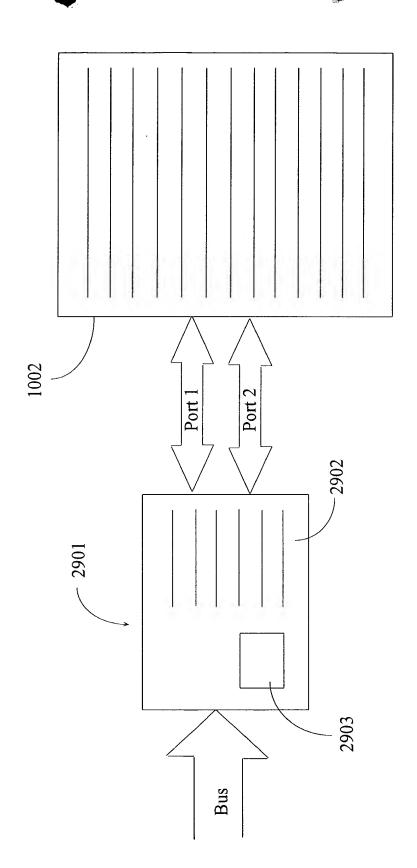


Fig. 29